Scalable Complementary Logic Gates with Chemically Doped Semiconducting Carbon Nanotube Transistors

Si Young Lee, Sang Won Lee, Soo Min Kim, Woo Jong Yu, Young Woo Jo, and Young Hee Lee*

BK21 Physics Division, Department of Energy Science, and Center for Nanotubes and Nanostructured Composites, Sungkyunkwan Advanced Institute of Nanotechnology, Sungkyunkwan University (SKKU), Suwon 440-746, Korea

ABSTRACT Use of random network carbon nanotube (CNT) transistors and their applications to complementary logic gates have been limited by several factors such as control of CNT density, existence of metallic CNTs producing a poor yield of devices, absence of stable n-dopant and control of precise position of the dopant, and absence of a scalable and cost-effective fabrication process. Here, we report a scalable and cost-effective fabrication of complementary logic gates by precisely positioning an air-stable n-type dopant, viologen, by inkjet printing on a separated semiconducting CNTs network. The obtained CNT transistors showed a high yield of nearly 100% with an on/off ratio of greater than 10^3 in an optimized channel length ($\sim$9 μm). The n-doped semiconducting carbon nanotube transistors showed a nearly symmetric behavior in the on/off current and threshold voltage with p-type transistors. CMOS inverter, NAND, and NOR logic gates were integrated on a HfO_2/Si substrate using the n/p transistor arrays. The gain of inverter is extraordinarily high, which is around 45, and NAND and NOR logic gates revealed excellent output on and off voltages. These series of whole processes were conducted under ambient conditions, which can be used for large-area and flexible thin film technology.

KEYWORDS: random network CNT array · semiconducting carbon nanotubes · chemical *n*-doping · inkjet printing · CMOS logic gates · high yield

Carbon nanotubes (CNTs) have been extensively investigated for transistors owing their high mobility of $\sim$10000 cm^2 V^{-1} s^{-1} and the potential for high integration circuits for future electronics.[1−4] Several complicated logic gates such as inverter, NAND, NOR, and ring oscillator have been demonstrated so far using individual CNTs or random network CNTs.[5−8] Nevertheless, the device performance has been limited by several fundamental factors, let alone the scalability to industrialization: (i) assembly of individual CNTs in a desired position in the circuit, (ii) existence of metallic CNTs in the pristine CNTs, (iii) difficulty in doping control, in particular stable n-type doping under ambient conditions, and (iv) large hysteresis.

Although an individual carbon nanotubes field effect transistor (CNT-FET) demonstrates high on/off ratio and mobility,[4,6] fabrication of such an individual device has been extremely inefficient from a technology point of view, let alone the integration of such devices into arrays. Another alternative approach is a random network CNT transistor. There are several ways to fabricate network channels of transistors such as dielectrophoresis, spray, inkjet printing, self-assembly, and *in situ* chemical vapor deposition (CVD). Dispersed CNTs in solution have been used for dielectrophoresis to self-assembly under ambient conditions, while CNTs from *in situ* CVD were grown directly on a substrate at high temperature. Several obstacles still exist in these approaches. Dielectrophoresis is used for alignment of the CNT network along the channel. However, this method is quite inefficient to get a high yield in array structures.[9] The spray method uses the CNT solution but is not widely applied due to the difficulty in finding optimized conditions.[10] Inkjet printing is advantageous for the positioning of the channels within a reasonable resolution and large area applications, but the fabrication speed is relatively slow, and moreover it is not easy to find the optimum conditions for high device performance.[11] Another technique is a self-assembly method where CNTs can be self-assembled on a functionalized substrate, but controllability of CNT density in the channel is extremely difficult.[12] The *in situ* CVD is not compatible under low temperature, and otherwise an additional transfer process of CNTs is required.[13]

The presence of metallic CNT channels in a random network transistor degrades the on/off ratio. The metallic channels are burned out by applying a high voltage,

* Address correspondence to leeyoung@skku.edu.

Received for review January 22, 2011 and accepted February 14, 2011.

Published online March 03, 2011
10.1021/nn200270e

© 2011 American Chemical Society

which requires an extra process.[14−16] Recently, to overcome this difficulty, separated semiconducting CNTs have been used for transistors.[12,17,18] The on/off ratio was improved, while the mobility ranged from 1 to 10 $cm^2 V^{-1} s^{-1}$, not better than those obtained from mixed CNTs. In general, on/off ratio and mobility are complementary to each other. This trade-off characteristic also relies on the CNT density in a random network transistor. For instance, at low coverage of CNTs, a high on/off ratio is expected but low on current and mobility are expected, whereas at high coverage of CNTs, high mobility is expected but a low on/off ratio due to the increased chances of having a metallic network is expected. Use of the separated semiconducting CNTs is certainly advantageous for a random network transistor, but careful optimization is required to overcome this trade-off characteristic.

Another critical issue for high performance complementary metal-oxide-semiconductor (CMOS) CNT logic gates is a matching of p-type and n-type FET. The CNT transistor shows p-type behavior under ambient conditions. The n-type transistor has been realized by the doping of electron-donating groups such as potassium, polyethyleneimine (PEI), and hydrazine.[19−21] However, these are usually unstable under ambient conditions. For this reason, the PMOS logic gate using a p-type transistor and a resistor (or only p-type transistors) has been demonstrated. This circuit, however, maintains DC current flow whenever the p-type transistor is on, giving rise to static power consumption. Low work function metals such as aluminum, calcium, or scandium have been introduced to realize a n-type transistor.[6,22−24] Again, such electrodes can be easily oxidized under ambient conditions, which is not compatible with an ambient fabrication process, and need additional photolithography processes. Recently, stable n-type doping has been realized using electron-donating viologen and NADH.[25,26] This provides an opportunity to develop realistic n/p CMOS logic gates.

The purpose of this paper is to develop a scalable process for n/p CMOS logic gates by optimizing the device performance and incorporating chemical n-type doping by inkjet printing with separated semiconducting single-walled carbon nanotubes (SWCNTs) under ambient conditions. The separated SWCNTs with 95% semiconducting CNTs were spin-casted on HfO_2 (thickness: 50 nm)/Si substrate followed by a photolithography of forming electrodes of 576 devices on 3×3 cm^2. The n-type doping was realized by inkjet printing viologen solution on the channel of the desired devices. This gave rise to the similar level of on/off current to p-type transistor and well separated threshold voltage, which are necessary to construct n/p CMOS logic gates with high performance. High yield of 99% was achieved with an average on/off ratio of 10^2-10^6, a mobility of 1−10 $cm^2 V^{-1} s^{-1}$, a hysteresis of around 2 V, and low operation voltage less than ±5 V. The fabricated inverter, NAND, and NOR logic gates revealed excellent output on and off voltages with an inverter gain of around 45 at V_{dd} = 2 V.

RESULTS AND DISCUSSION

Figure 1a shows an optical image of the device array whose channel lengths are 3, 5, 7, and 9 μm and channel widths are 10, 20, and 30 μm. The right panels show the spin-casted random network SWCNTs at different amounts of CNT solutions. A higher density of CNT network was obtained in 100 μL. The difference in the CNT density indicates the controllability of the spin coating process with determined CNT solution. SWCNTs were well dispersed without bundle formation, as expected from the well-dispersed SWCNT solution shown in the inset, which is necessary to obtain a high on/off ratio. The pristine SWCNT transistor on HfO_2/Si substrate shows p-type behavior (blue line), whereas the viologen-doped transistor shows clearly n-type behavior (red line) in Figure 1b. On-current levels for both types were similar to each other, and moreover the threshold voltages for both types were well separated, which is essential for the operation of high performance logic gates. In addition, these transistors showed small hysteresis (~2 V) as well as low operating gate voltage within ±3 V so that the power consumption is low. Therefore, the use of a high-κ dielectric material, HfO_2, gave better device performances than the use of a low-κ dielectric material such as SiO_2.[12,27] For logic gates, the bottom gate lines of Cr/Au were patterned directly on SiO_2/Si. Then, HfO_2, approximately 50 nm, was deposited on the substrate by atomic layer deposition. Source−drain lines of Cr/Au were then patterned on HfO_2 after the spin coating of the CNT solution, as shown in Figure 1c and 1d. As a final step, the viologen solution was selectively dropped for n-type doping on the desired channels by inkjet printing, which was a necessary step to resolve a problem that photoresist can be melted easily in viologen-dissolved toluene.

Figure 2a shows typical transfer characteristics of the thin-film transistors (TFTs) prepared with 100 and 75 μL CNT solutions. Although the absolute on and off currents varied from sample to sample, these two curves represent the average values for two solution amounts. On and off currents were large in the case of 100 μL compared to those of 75 μL due to more available CNT channels. The on/off ratio was better in the case of 75 μL compared to that of 100 μL due to less chance of metallic channels. This reflects that the remaining 5% metallic CNTs still affect the channel characteristics. A complete removal of metallic CNTs is necessary to improve the on/off ratio. The source−drain currents of 100 μL were well modulated with gate voltages within ±1 V_{DS} range in Figure 2b. The linear curves indicate an ohmic contact between metal and

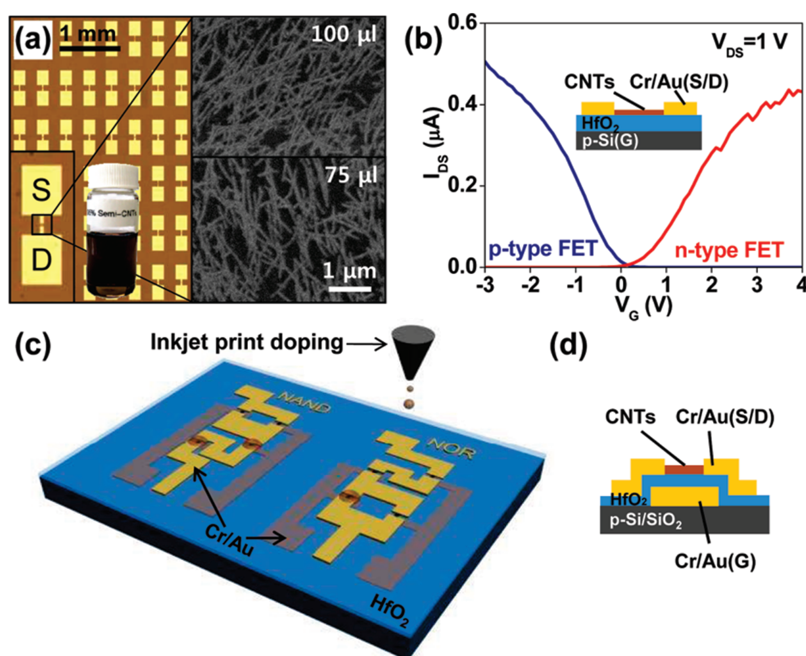

Figure 1. (a) Optical image of transistor array which is composed of 144 × 4 transistors on 3 × 3 cm^2 HfO_2/Si substrate. Channel lengths are 3, 5, 7, 9 μm and channel widths are 10, 20, 30 μm. The source and drain electrodes are magnified in the inset. Another inset shows a bottle of the CNT solution. The morphology of SWCNTs network is shown in the right panel with different amounts of SWCNT solutions. (b) Typical transfer characteristics of p-type (blue) and n-type (red) transistors at V_{DS} = 1 V. Side view of backgate structure is shown in the inset. (c) The logic circuits layout and (d) a side view of an individual transistor in the logic gate.

CNTs. The currents started saturating at 2 V, similar to typical Si transistors as shown in the inset of Figure 2b. The distribution of on/off ratios in 288 TFTs are shown in Figure 2c. Most devices of more than 99% were operated without disconnection. A higher on/off ratio was obtained in the case of 75 μL. Accumulative yield shows a high yield of nearly 100% with an on/off ratio of greater than 10^3 at a channel length of 9 μm and a solution density of 75 μL. The on/off ratio also depends on the channel length in Figure 2d. At a low CNT density of 75 μL, the on/off ratio increased linearly with channel length, whereas at a high CNT density of 100 μL, the on/off ratio increased to saturate at a long channel length. Chances of increasing semiconducting CNT channels increase with channel length, but at high CNT concentration this value simply saturates due to the average effect of such channels. This phenomenon is in agreement with the previous reports.[3,11,12] Figure 2e shows the graph for mobility *versus* on/off ratio. The mobility was calculated by the equation of $\mu = (Lg_m)/(WC_{ox}V_{DS})$, where L is the channel length, g_m (= dI_{DS}/dV_G) is the maximum transconductance, W is the channel width, C_{ox} (= $\varepsilon_0\varepsilon_{ox}/t_{ox}$) is the gate capacitance per unit area, and V_{DS} is the applied drain−source voltage. At a low CNT density of 75 μL, the on/off ratio was high, whereas the average mobility was low at about 2 cm^2 V^{-1} s^{-1}. At a high CNT density of 100 μL, the on/off ratio was reduced, but the mobility increased up to 10 cm^2 V^{-1} s^{-1}. Although the data points were scattered in a wide region, there is a tendency for the mobility to decrease with increasing on/off ratio. This phenomenon is caused by the increase of the conducting path length from the presence of 5% metallic CNTs. Thus, 5% metallic nanotubes can contribute to the increase of mobility even though this density degrades the on/off ratio. The resistance increased linearly with increasing channel length, as shown in Figure 2f. An extrapolation of the linear slope to zero channel length provides the contact resistance. Higher CNT density gave rise to smaller contact resistance owing to the formation of more parallel resistances of CNTs.

The n-type doping was realized by dropping the prepared viologen solution on a desired channel by inkjet printing after fabrication of the device array. With n-type doping, the threshold voltage was shifted toward the positive bias region, and the complete type conversion was realized with a similar on/off ratio to the pristine p-type FET (75 μL), as shown in Figure 3a. Channel length and width of both p- and n-type transistors were 9 and 10 μm, respectively. Furthermore, the off-current was low enough (10^{-10} A) to be compatible with Si TFTs.[28,29] The typical source−drain curve of the n-type FET was shown with a clear gate modulation with gate bias in Figure 3b, again demonstrating an ohmic behavior at a low voltage region and saturation behavior at a higher voltage region (inset). The threshold voltages of 9 × 2 representative samples were scattered again stochastically in Figure 3c. Nevertheless, a clear distinction between p-type and n-type transistors was observed. While negative threshold voltages were observed in p-type FETs, positive

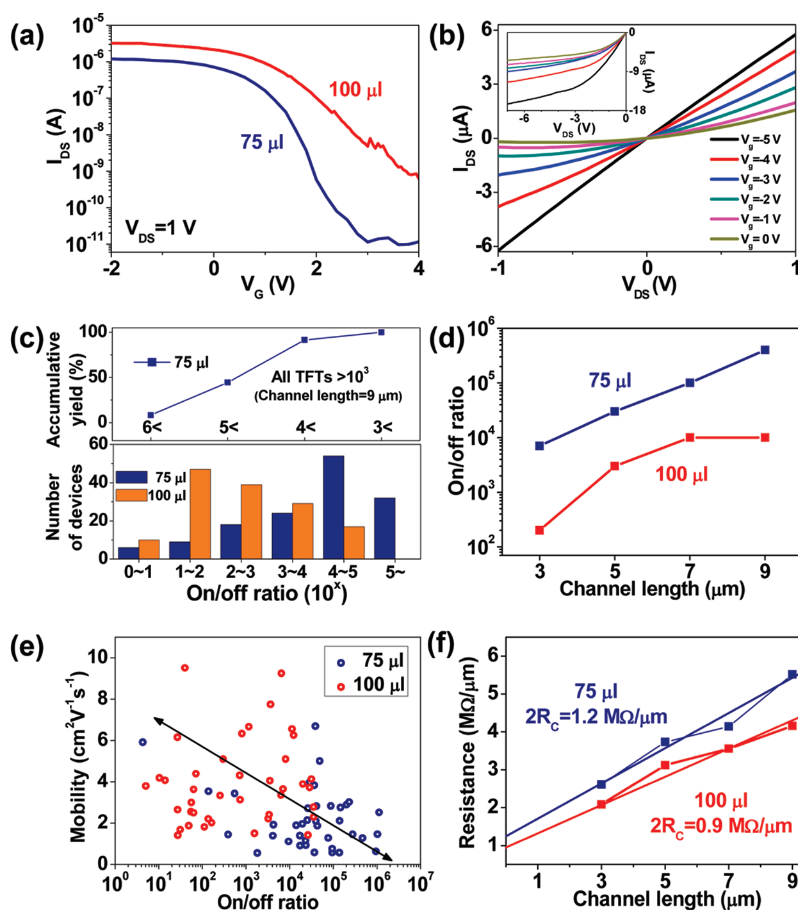

Figure 2. Characteristics of p-type FET with different amounts of CNT solution. (a) Typical transfer characteristics at V_{DS} = 1 V for a given CNT solution amount at a channel length of 9 μm. (b) $I_{DS}-V_{DS}$ characteristics in terms of gate voltage (100 μL). The inset shows saturation behavior at high voltage. (c) Statistics of the number of devices with different on/off ratios and accumulative yield for each number. (d) Average on/off ratio as a function of channel length measured at V_{DS} = 1 V. (e) Mobility *vs* on/off ratio. (f) Resistance as a function of channel length.

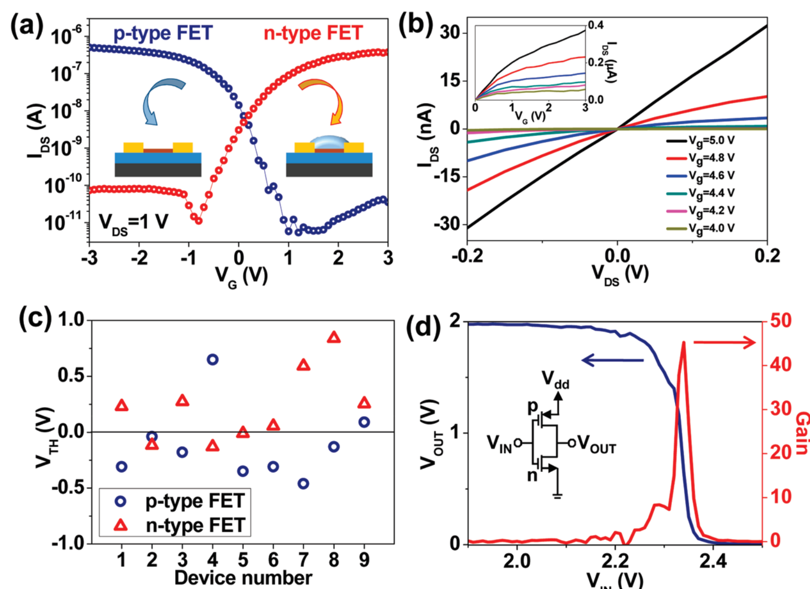

Figure 3. (a) $I_{DS}-V_G$ characteristics of p-type and n-type transistors at V_{DS} = 1 V (75 μL). Side view of both types is shown in the inset. (b) $I_{DS}-V_{DS}$ characteristics of n-type transistor in terms of gate voltage (75 μL). The inset shows saturation behavior at high voltage. (c) Threshold voltage of p-type (blue) and n-type (red) transistors; 9 × 2 representative transistors were measured. (d) Output characteristic and gain (~45) of inverter at V_{dd} = 2 V constructed with p-type and n-type transistors from panel a. Structure of inverter is shown in the inset.

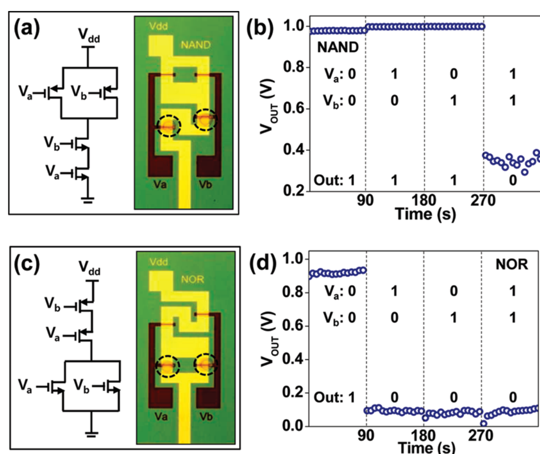

Figure 4. Structure and output characteristics of CMOS NAND and NOR logic gate. Schematic and optical image of (a) NAND and (C) NOR gates design directly on SiO_2/Si substrate. Viologen inkjet doping areas are marked with dashed circles in the optical image. Output characteristics of (b) NAND and (d) NOR gate at V_{dd} = 1 V, and two input voltages, V_a and V_b, are 0 V for logical 0 and 5 V for logical 1.

threshold voltages were observed in n-type FETs. The shift of the threshold voltage in n-type FETs results from the shift of the Fermi level toward the conduction band due to the donating charges from viologen to CNTs. The separated threshold voltage in the two different regions does not invoke power consumption owing to no simultaneous opening of two transistors. By combining two n/p FETs, the complementary inverter was fabricated, as shown in the inset of Figure 3d. The viologen was selectively dropped on the bottom transistor in the inverter circuit by inkjet printing (inset of Figure 3d). Transistors obtained from 75 μL CNT solution were used for all logic gates because of their high on/off ratio. With V_{dd} = 2 V, clear output on (2 V) and off (0 V) states were observed. These clear output characteristics were realized by a small leakage current at the off state of p- and n-type transistors. It is interesting to note that a high gain of 45 was obtained in our case, while typical gains have been observed around 10 at V_{dd} = 2 V in the previous results of the network-type CNT inverter.[30,31]

The precise positioning of the n-type doping on the desired channels by inkjet printing allowed us to fabricate more robustly complex CMOS NAND and NOR logic gates. For this purpose, Cr/Au was deposited as the back gates, as described in Figure 1d, while the rest of the fabrication processes were the same as individual transistors. The dashed circles in the optical image in Figure 4a,c indicate n-type transistors that were selectively doped by viologen inkjet printing. The NAND circuit with 2 p-type transistors in parallel and 2 n-type transistors in series was shown in Figure 4a. The typical output characteristics of CMOS NAND gate with three clear on-outputs for either V_a or V_b to be clearly zero and one off-output for $V_a = V_b = 5$ V at $V_{dd} = 1$ V were shown in Figure 4b. Similar structures were also shown for a CMOS NOR gate in Figure 4c,d. The NOR gate consists of 2 p-type transistors in series and 2 n-type transistors in parallel. One clear on and three clear off state outputs were realized with a combination of 1 or 0 in V_a and V_b input at $V_{dd} = 1$ V.

CONCLUSION

We fabricated high-performance complementary logic gates by using random network semiconducting carbon nanotube (purity of 95%) transistor arrays. A high yield of nearly 100% with excellent device performance of mobility of up to 10 cm^2 V^{-1} s^{-1}, or on/off ratio of greater than 10^3, was realized by optimizing CNT solution density and channel length. With a precise control of positioning air-stable n-type dopant of viologen on a desired channel by inkjet printing, nearly symmetric behaviors in the on/off current and a threshold voltage between p-type and n-type transistors were obtained. This led to integrate complicated CMOS logic gates such as inverter, NAND, and NOR gates, which revealed a high inverter gain of around 45 and excellent on and off states in the output. These high performance devices and stable n-type doping by inkjet print are readily scalable under ambient conditions, which can lead to large-area and flexible thin-film technology for future electronics.

MATERIALS AND METHODS

Preparation of CNTs Solution. The semiconducting CNTs which contain 95% semiconducting CNTs were purchased from Iso-Nanotubes-S 95%, Nanointegris, USA. The CNT powder of 0.3 mg was dissolved and sonicated in 1-methyl-2-pyrrolidinone (NMP: 99+%, spectrophotometric grade, Sigma Aldrich) of 30 mL for 2.5 h in a bath-type sonicator (RK 106, Bandelin Electronic, Germany) to get a CNT concentration of 10 μg/mL. The mixed solution was centrifuged to remove the remaining bundles in the solution at 13000 rpm for 2 h (Mega 17R, Hanil Science Industrial Co., Ltd.). This solution was used for spin coating CNT channels.

HfO_2 Deposition by ALD. The p-Si wafer was immersed into piranha solution (H_2O_2/H_2SO_4 = 1:3) for 30 min and then flushed by distilled water. After cleaning the wafer, the commercial atomic layer deposition (ALD) apparatus (Lucida D100, NCD Technology, Korea) was used for HfO_2 deposition at 200 °C. One cycle consists of an alternative supply of HfO_2 (TEMAHf) and water precursors. HfO_2 precursor was supplied first with N_2 carrier gas for 1 s and purged with N_2 gas only for 10 s. Water precursor was then supplied with N_2 gas for 0.5 s and purged again to remove the residual HfO_2 precursor for 10 s. One cycle gives rise to a HfO_2 thickness of around 0.1 nm. This was repeated for 500 cycles to get an oxide thickness of around 50 nm. Capacitance−voltage measurement was used to estimate the dielectric constant, which was around 15.

Fabrication of Individual TFTs. Before spin coating of CNTs, a HfO_2/Si wafer was immersed into 2.5 mM of

3-aminopropyltriethoxysilane (APTES: 99%, Sigma Aldrich) which was diluted in distilled water for 30 min. The functionalized wafer was then used to spin coat the CNTs. Two different volumes of 75 μL and 100 μL were spin coated at 4000 rpm in this study. The CNT-coated HfO_2/Si wafer was dried by a dry oven at 70 °C for 1.5 h. Conventional photolithography and e-beam/thermal evaporator were used to make an electrode pattern with Cr/Au (5 nm/50 nm). The electrode pattern has channel lengths of 3, 5, 7, 9 μm and channel widths of 10, 20, 30 μm. The CNTs, except channel area, were etched away by O_2 plasma by RIE (Miniplasma-Cube, Plasmart) at 20 W for 10 s by using a patterned photoresist from photolithography.

Fabrication of CMOS NAND and NOR. For NAND and NOR, the SiO_2 (300 nm)/p-Si wafer was cleaned by piranha solution. In this case, an individual back gate of 5 nm/30 nm of Cr/Au was patterned by photolithography and a lift-off process on the wafer. The rest of the processes of depositing HfO_2 and CNTs were the same as those of individual TFTs. An additional deposition of source, drain, and interconnections (Cr/Au 5 nm/50 nm) was evaporated. Unnecessary CNTs except channel area were removed by O_2 plasma etching by RIE. Finally, 100 mM of viologen was dropped to create an n-doped transistor by inkjet printer (UJ-500 MF, Unijet) after annealing it in oven (200 °C for 1 h in vacuum).

Measurements. The degree of dispersion was evaluated by UV−vis−NIR absorption spectroscopy (Cary 5000, Varian). FES-EM (JSM 7000F, JEOL) was used to observe the morphology of the coated CNTs on the wafer. Semiconductor characterization system (4200-SCS, Keithley) was used for the electrical measurements.

Acknowledgment. This study was supported by the STAR-faculty program and WCU (World Class University) program through the KRF funded by the MEST (R31-2008-000-10029-0), the Industrial Technology Development Program (10031734) of the Ministry of Knowledge Economy (MKE), Samsung Mobile Display Co., and the IRDP of NRF (2010-00429) through a grant provided by MEST in 2010 in Korea.

REFERENCES AND NOTES

1. Zhou, X.; Park, J. Y.; Huang, S.; Liu, J.; McEuen, P. L. Band Structure, Phonon Scattering, and the Performance Limit of Single-Walled Carbon Nanotube Transistors. *Phys. Rev. Lett.* **2005,** *95*, 146805/1–4.
2. Kang, S. J.; Kocabas, C.; Ozel, T.; Shim, M.; Pimparkar, N.; Alam, M. A.; Rotkin, S. V.; Rogers, J. A. High-Performance Electronics Using Dense, Perfectly Aligned Arrays of Single-Walled Carbon Nanotubes. *Nat. Nanotechnol.* **2007,** *2*, 230–236.
3. Yu, W. J.; Kim, U. J.; Kang, B. R.; Lee, I. H.; Lee, E. H.; Lee, Y. H. Adaptive Logic Circuits with Doping-free Ambipolar Carbon Nanotube Transistors. *Nano Lett.* **2009,** *9*, 1401–1405.
4. Franklin, A. D.; Chen, Z. Length Scaling of Carbon Nanotube Transistors. *Nat. Nanotechnol.* **2010,** *5*, 858–862.
5. Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, P. Carbon Nanotube Inter- and Intramolecular Logic Gates. *Nano Lett.* **2001,** *1*, 453–456.
6. Chen, Z.; Appenzeller, J.; Lin, Y. M.; Oakley, J. S.; Rinzler, A. G.; Tang, J.; Wind, S. J.; Solomon, P. M.; Avouris, P. An Integrated Logic Circuit Assembled on a Single Carbon Nanotube. *Science* **2006,** *311*, 1735.
7. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic Circuits with Carbon Nanotube Transistors. *Science* **2001,** *294*, 1317–1320.
8. Cao, Q.; Xia, M. G.; Shim, M. S.; Rogers, J. A. Bilayer Organic−Inorganic Gate Dielectrics for High-Performance, Low-Voltage, Single-Walled Carbon Nanotube Thin-Film Transistors, Complementary Logic Gates, and p-n Diodes on Plastic Substrates. *Adv. Funct. Mater.* **2006,** *16*, 2355–2362.
9. Li, J.; Zhang, Q.; Yang, D.; Tian, J. Fabrication of Carbon Nanotube Field Effect Transistors by AC Dielectrophoresis Method. *Carbon* **2004,** *42*, 2263–2267.
10. Artukovic, E.; Kaempgen, M.; Hecht, D. S.; Roth, S.; Grüner, G. Transparent and Flexible Carbon Nanotube Transistors. *Nano Lett.* **2005,** *5*, 757–760.
11. Okimoto, H.; Takenobu, T.; Yanagi, K.; Miyata, Y.; Shimotani, H.; Kataura, H.; Iwasa, Y. Tunable Carbon Nanotube Thin-Film Transistors Produced Exclusively *via* Inkjet Printing. *Adv. Mater.* **2010,** *22*, 3981–3986.
12. Wang, C.; Zhang, J.; Ryu, K.; Badmaev, A.; Arco, L. G. D.; Zhou, C. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009,** *9*, 4285–4291.
13. Min, Y. S.; Bae, E. J.; Oh, B. S.; Kang, D. H.; Park, W. J. Low-Temperature Growth of Single-Walled Carbon Nanotubes by Water Plasma Chemical Vapor Deposition. *J. Am. Chem. Soc.* **2005,** *127*, 12498–12499.
14. Collins, P. G.; Arnold, M. S.; Avouris, P. Engineering Carbon Nanotubes and Nanotube Circuits Using Electrical Breakdown. *Science* **2001,** *292*, 706–709.
15. Chiu, P. W.; Chen, C. H. High-Performance Carbon Nanotube Network Transistors for Logic Applications. *Appl. Phys. Lett.* **2008,** *92*, 063511/1–3.
16. Wang, C.; Ryu, K.; Badmaev, A.; Patil, N.; Lin, A.; Mitra, S.; Wong, H. −S. P; Zhou, C. Device Study, Chemical Doping, and Logic Circuits Based on Transferred Aligned Single-Walled Carbon Nanotubes. *Appl. Phys. Lett.* **2008,** *93*, 033101/1–3.
17. Engel, M.; Small, J. P.; Steiner, M.; Freitag, M.; Green, A. A.; Hersam, M. C.; Avouris, P. Thin Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays. *ACS Nano* **2008,** *2*, 2445–2452.
18. Fu, D.; Okimoto, H.; Lee, C. W.; Takenobu, T.; Iwasa, Y.; Kataura, H.; Li, L. J. Ultrasensitive Detection of DNA Molecules with High On/Off Single-Walled Carbon Nanotube Network. *Adv. Mater.* **2010,** *22*, 4867–4871.
19. Zhou, C.; Kong, J.; Yenilmez, E.; Dai, H. Modulated Chemical Doping of Individual Carbon Nanotubes. *Science* **2000,** *290*, 1552–1555.
20. Shim, M.; Ali, J.; Kam, N. W. S.; Dai, H. Polymer Functionalization for Air-Stable n-Type Carbon Nanotube Field-Effect Transistors. *J. Am. Chem. Soc.* **2001,** *123*, 11512–11513.
21. Klinke, C.; Chen, J.; Afzail, A.; Avouris, P. Charge Transfer Induced Polarity Switching in Carbon Nanotube Transistors. *Nano Lett.* **2005,** *5*, 555–558.
22. Nosho, Y.; Ohno, Y.; Kishimoto, S.; Mizutani, T. n-Type Carbon Nanotube Field-Effect Transistors Fabricated by Using Ca Contact Electrodes. *Appl. Phys. Lett.* **2005,** *86*, 073105/1–3.
23. Nosho, Y.; Ohno, Y.; Kishimoto, S.; Mizutani, T. Relation Between Conduction Property and Work Function of Contact Metal in Carbon Nanotube Field-Effect Transistors. *Nanotechnology* **2006,** *17*, 3412–3415.
24. Zhang, Z.; Liang, X.; Wang, S.; Yao, K.; Hu, Y.; Zhu, Y.; Chen, Q.; Zhou, W.; Li, Y.; Yao, Y.; *et al.* Doping-free Fabrication of Carbon Nanotube Based Ballistic CMOS Devices and Circuits. *Nano Lett.* **2007,** *7*, 3603–3607.
25. Kang, B. R.; Yu, W. J.; Kim, K. K.; Park, H. K.; Kim, S. M.; Park, Y.; Kim, G.; Shin, H. J.; Kim, U. J.; Lee, E. H.; *et al.* Restorable Type Conversion of Carbon Nanotube Transistor Using Pyrolytically Controlled Antioxidizing Photosynthesis Coenzyme. *Adv. Funct. Mater.* **2009,** *19*, 2553–2559.
26. Kim, S. M.; Jang, J. H.; Kim, K. K.; Park, H. K.; Bae, J. J.; Yu, W. J.; Lee, I. H.; Kim, G.; Duong, D. L.; Kim, U. J.; *et al.* Reduction-Controlled Viologen in Bisolvent as an Environmentally Stable n-Type Dopant for Carbon Nanotubes. *J. Am. Chem. Soc.* **2009,** *131*, 327–331.
27. Yang, M. H.; Teo, K. B. K.; Gangloff, L.; Milne, W. I.; Hasko, D. G.; Robert, Y.; Legagneux, P. Advantages of Top-Gate, High-κ Dielectric Carbon Nanotube Field-Effect Transistors. *Appl. Phys. Lett.* **2006,** *88*, 113507/1–3.
28. Chiang, C. S.; Kanicki, J.; Takechi, K. Electrical Instability of Hygrogenated Amorphous Silicon Thin-Film Transistors for Active-Matrix Liquid−Crystal Displays. *Jpn. J. Appl. Phys.* **1998,** *37*, 4704–4710.
29. Martin, S.; Chiang, C. S.; Nahm, J. Y.; Li, T.; Kanicki, J.; Ugai, Y. Influence of the Amorphous Silicon Thickness on Top

Gate Thin-Film Transistor Electrical Performances. *Jpn. J. Appl. Phys.* **2001,** *40*, 530–537.
30. Nouchi, R.; Tomita, H.; Ogura, A.; Kataura, H.; Shiraishi, M. Logic Circuits Using Solution-Processed Single-Walled Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2008,** *92*, 253507/1–3.
31. Ryu, K. M.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H. −S. P.; Zhou, C. CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Intergrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009,** *9*, 189–197.